AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph starting at line 26 on page 10 as follows:

Namely, as shown in a principle (1) of a packet processing device 10 according to the present invention of Fig. 1, a second means, i.e. a reassembly buffer processor 301 in a lower layer protocol processor 300 reassembles plural receiving packets 91 into a single big packet 92. In this case, a third means, i.e. an accumulation condition-determining portion 303 determines the size of the big packet 92 based on a free space 93 of a receiving buffer 101 from a first means, i.e. a receiving buffer free space notifying portion 102.

a1

Please amend the paragraph starting at line 6 on page 11 as follows:

It is to be noted that a layer in which the free space notifying portion 102 is allocated, as will be described later, is not necessarily an upper layer. Also, a receiving packet 90, a connection identifying circuit 302 and a checksum calculating circuit 304 shown in Fig. 1 will be described later. In the foregoing description, each of the receiving packets 91 and the receiving packet 90 are the same, since a connection of the receiving packet 90 is not identified.

a2

Please amend the paragraph starting at line 15 on page 12 as follows:

Fig. 3 shows a principle (3) of the present invention, in which the difference from Fig. 1 is that there is a middle layer protocol processor 200 between the upper layer protocol processor 100 and ~~a~~ the lower layer protocol processor 300.

a3

Please amend the first paragraph on page 13 as follows:

Namely, the connection identifying circuit 302 shown in Fig. 1 identifies the connection of the receiving packet 90 so that the reassembly buffer processor 301 can reassemble the receiving

a4

packet 91 resulting from the identification into the big packet 92 for each identical connection.